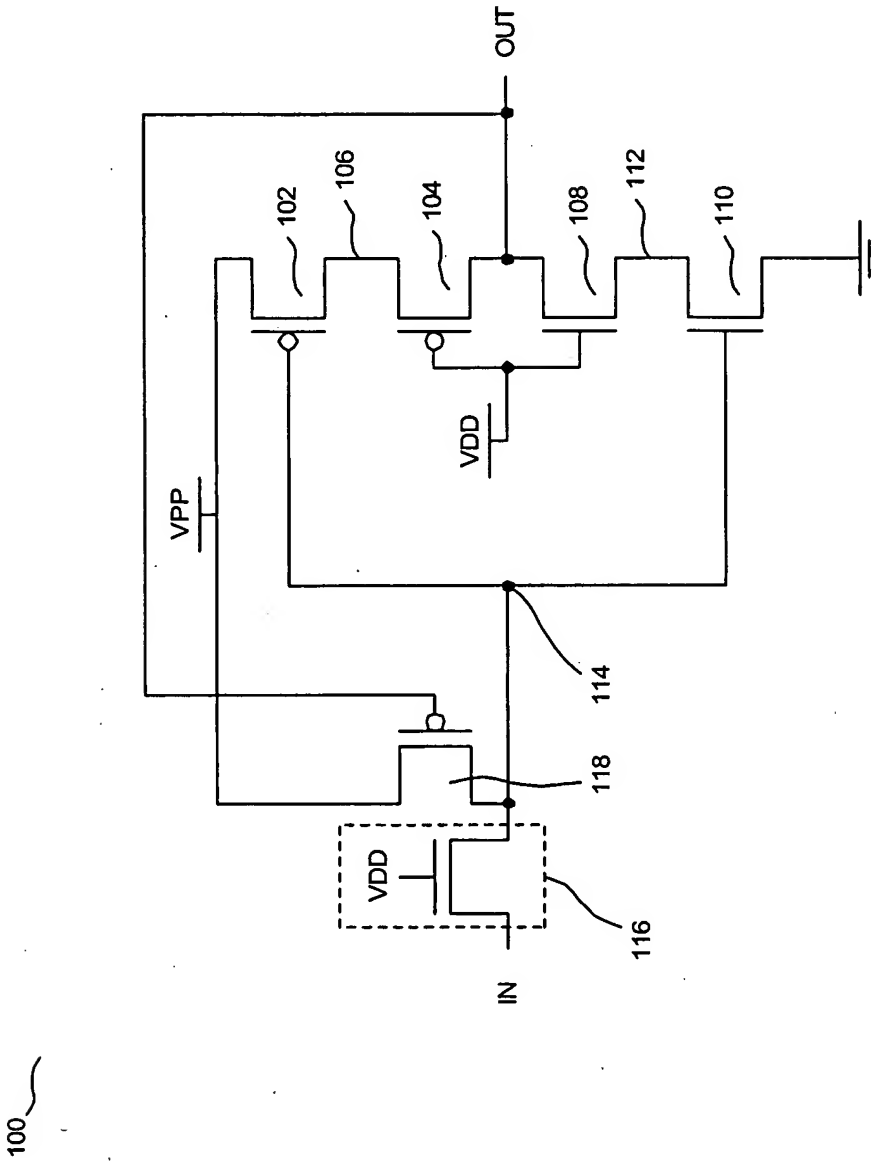

FIG. 1

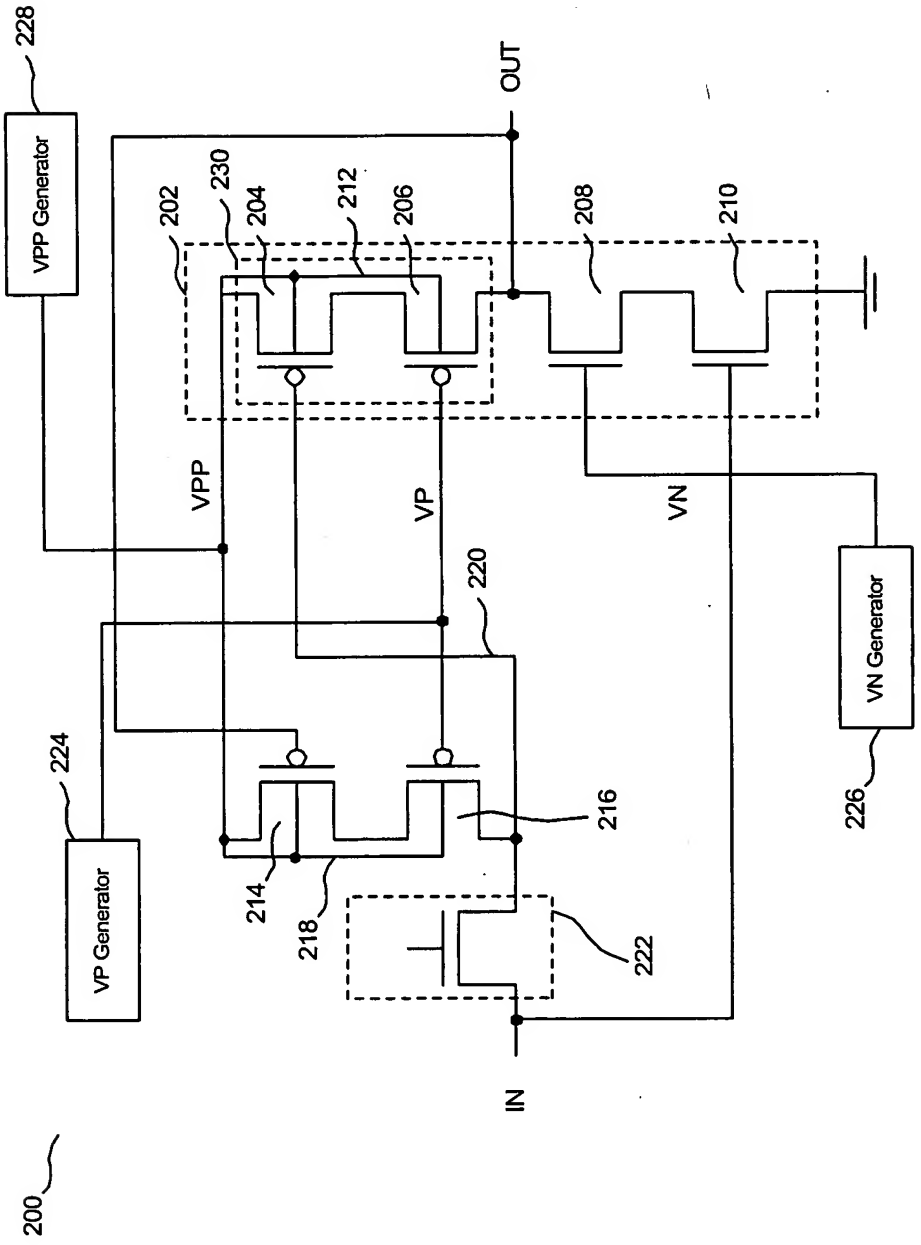
200
228
VPP Generator
OUT
202
230
204
212
206
208
210
VPP
VP
VN
220
224
VP Generator
214
218
216
222
VN Generator
226
IN

FIG. 2A

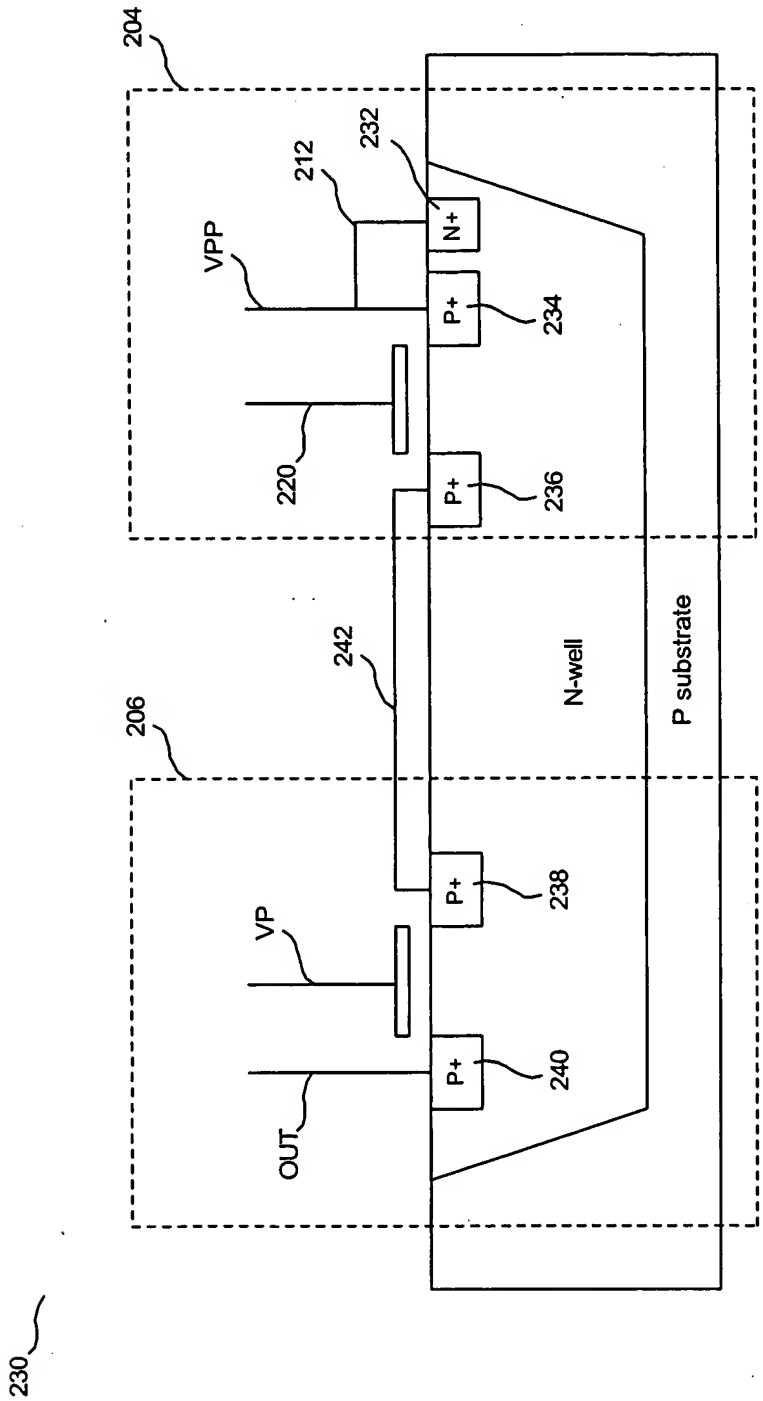
204
232
212
VPP
N+
P+
234
220
P+
236
242
206
N-well
P substrate
P+
238
VP
P+
240
OUT
230

FIG. 2B

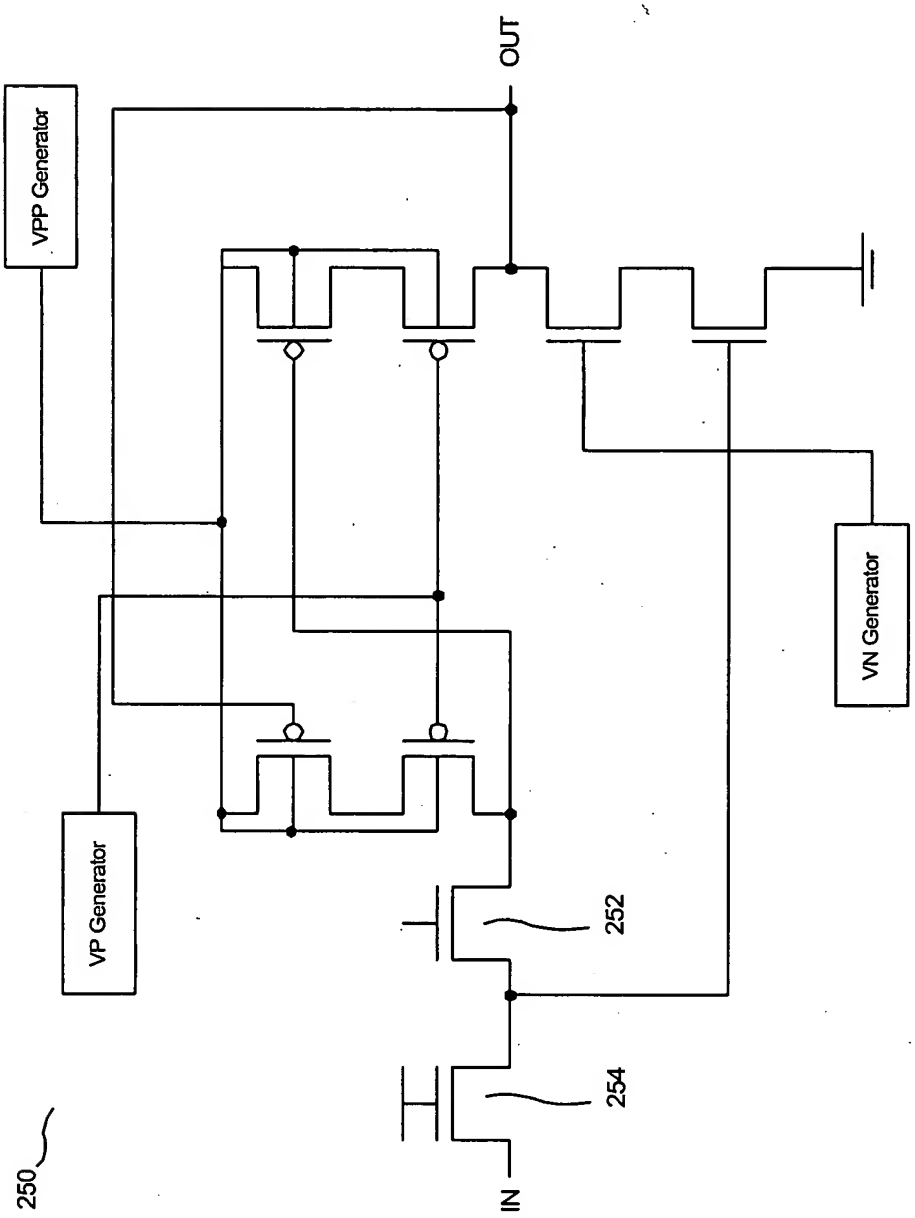

FIG. 2C

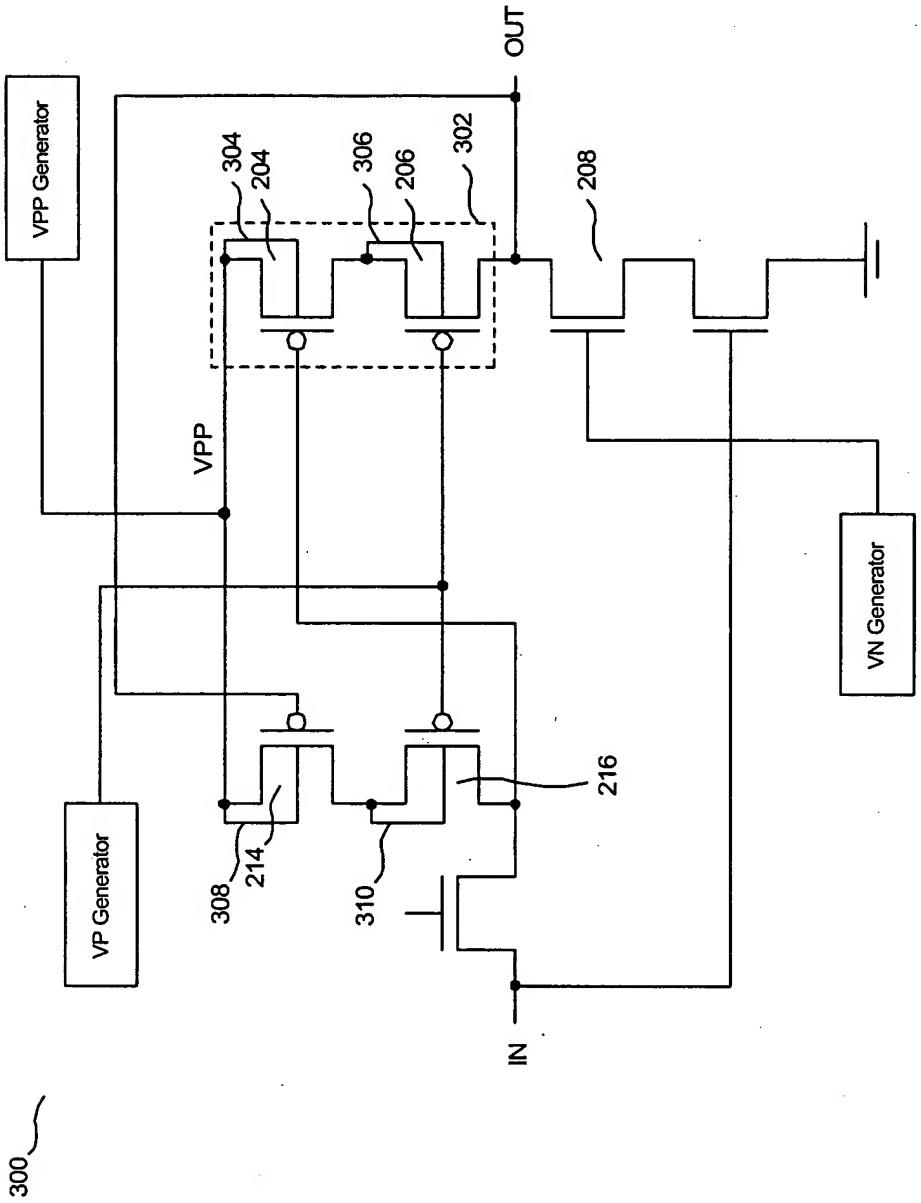
OUT
VPP Generator
304
204
306
206
302
208
VPP
VN Generator
216
VP Generator
308
214
310
IN
300

FIG. 3A

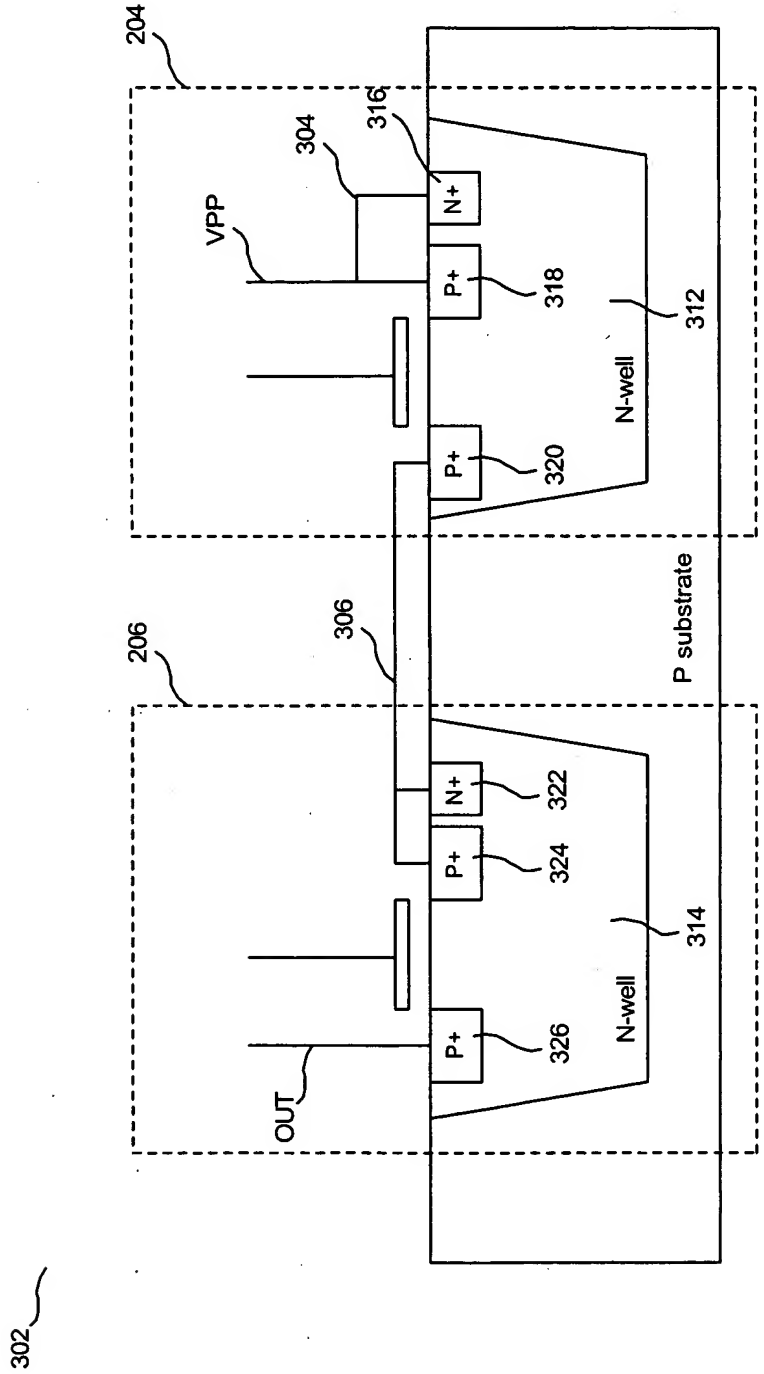
204
316
304
VPP
N+
P+
318
312
N-well
P+
320
306
206
P substrate
N+
322
P+
324
314
N-well
P+
326
OUT
302

FIG. 3B

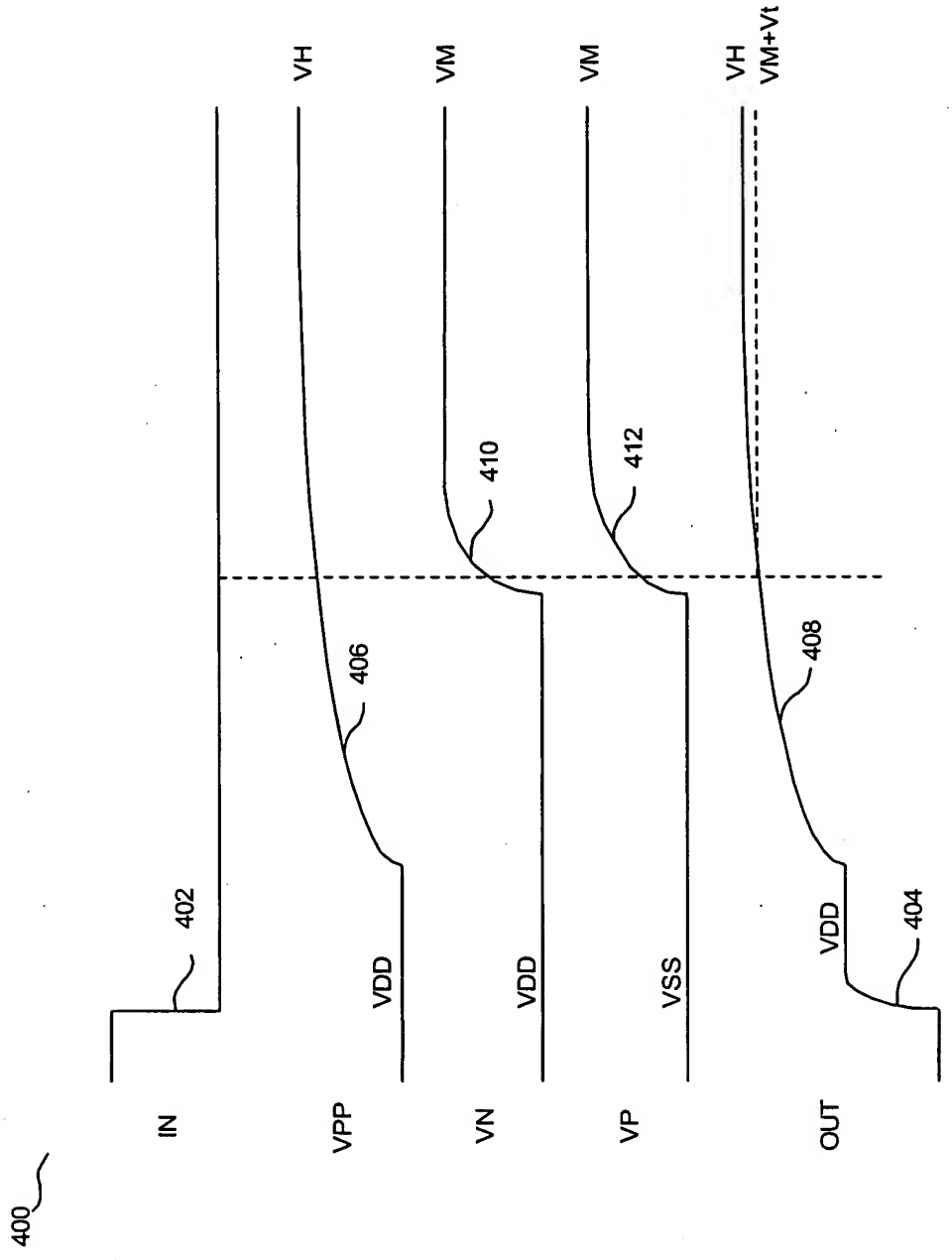
400
IN
VPP
VN
VP
OUT
VH
VM
VM
VH
VM+Vt
402
406
410
412
408
404
VDD
VDD
VSS
VDD

FIG. 4

500

Stress Voltage	Switch circuit 100	Switch circuit 300
drain to source (punch through)	< (VH - VDD + Vtn) for nMOS > - (VH - VDD + |Vtp|) for pMOS	< (VH - VM + Vtn) for nMOS > - (VH - VM + |Vtp|) for pMOS
drain to gate (gated breakdown)	VH - VDD for nMOS - (VH - VDD) for pMOS	VH - VM for nMOS - (VH - VM) for pMOS

FIG. 5A

502

Stress Voltage	Switch circuit 100	Switch circuit 300
drain to source (punch through)	< 11.7V for nMOS > -11.7V for pMOS	< 7.0V for nMOS > -7.0V for pMOS
drain to gate (gated breakdown)	11.2V for nMOS -11.2V for pMOS	6.5V for nMOS -6.5V for pMOS

FIG. 5B

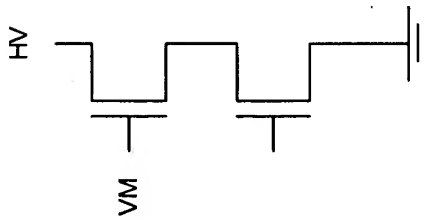

FIG. 6B

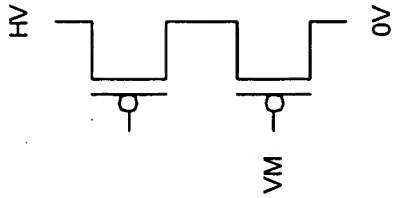

FIG. 6A